

CMLDM3757

**SURFACE MOUNT  
N-CHANNEL AND P-CHANNEL  
ENHANCEMENT-MODE  
COMPLEMENTARY MOSFETS**

PICOmini™



**SOT-563 CASE**

• Device is **Halogen Free** by design

**APPLICATIONS:**

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Devices

**MAXIMUM RATINGS:** ( $T_A=25^\circ\text{C}$ )

Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	8.0	V
Continuous Drain Current (Steady State)	$I_D$	540	430
Maximum Pulsed Drain Current ( $t_p=10\mu\text{s}$ )	$I_{DM}$	1500	750
Power Dissipation (Note 1)	$P_D$	350	mW
Power Dissipation (Note 2)	$P_D$	300	mW
Power Dissipation (Note 3)	$P_D$	150	mW
Operating and Storage Junction Temperature	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$
Thermal Resistance (Note 1)	$\theta_{JA}$	357	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS:** ( $T_A=25^\circ\text{C}$ )

SYMBOL	TEST CONDITIONS	N-CH (Q1)		P-CH (Q2)		UNITS
		MIN	MAX	MIN	MAX	
$I_{GSSF}, I_{GSSR}$	$V_{GS}=4.5\text{V}, V_{DS}=0$	-	5.0	-	2.0	$\mu\text{A}$
$I_{DSS}$	$V_{DS}=16\text{V}, V_{GS}=0$	-	1.0	-	1.0	$\mu\text{A}$
$BV_{DSS}$	$V_{GS}=0, I_D=250\mu\text{A}$	20	-	20	-	V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.45	1.0	0.45	1.0	V
$V_{SD}$	$V_{GS}=0, I_S=350\text{mA}$	-	1.2	-	1.2	V
$r_{DS(ON)}$	$V_{GS}=4.5\text{V}, I_D=540\text{mA}$	-	0.55	-	-	$\Omega$
$r_{DS(ON)}$	$V_{GS}=4.5\text{V}, I_D=430\text{mA}$	-	-	-	0.9	$\Omega$
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=500\text{mA}$	-	0.7	-	-	$\Omega$
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=300\text{mA}$	-	-	-	1.2	$\Omega$
$r_{DS(ON)}$	$V_{GS}=1.8\text{V}, I_D=350\text{mA}$	-	0.9	-	-	$\Omega$
$r_{DS(ON)}$	$V_{GS}=1.8\text{V}, I_D=150\text{mA}$	-	-	-	2.0	$\Omega$

- Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm<sup>2</sup>  
 (2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm<sup>2</sup>  
 (3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm<sup>2</sup>



www.centrasemi.com

**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CMLDM3757 consists of complementary N-Channel and P-Channel Enhancement-mode silicon MOSFETs designed for high speed pulsed amplifier and driver applications. These MOSFETs offer Very Low  $r_{DS(ON)}$  and Low Threshold Voltage.

**MARKING CODE: 3C7**

**FEATURES:**

- ESD Protection up to 2kV
- 350mW Power Dissipation
- Very Low  $r_{DS(ON)}$
- Low Threshold Voltage
- Logic Level Compatible
- Small, SOT-563 Surface Mount Package

R1 (22-September 2010)

CMLDM3757

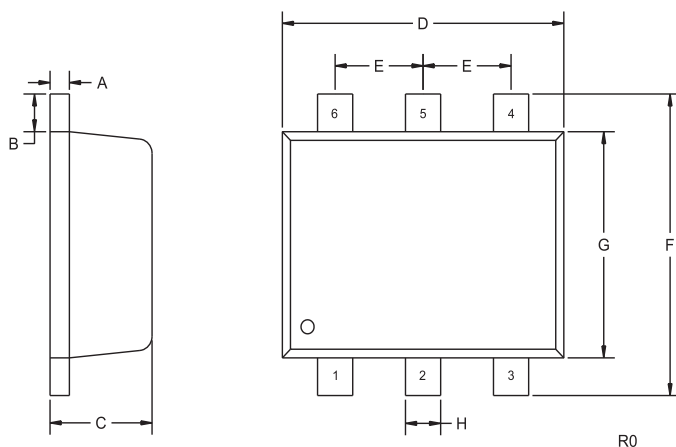
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N-CHANNEL AND P-CHANNEL  
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**ELECTRICAL CHARACTERISTICS - Continued:** ( $T_A=25^\circ\text{C}$ )

SYMBOL	TEST CONDITIONS	N-CH (Q1)		P-CH (Q2)		UNITS
		TYP	MAX	TYP	MAX	
$Q_G(\text{TOT})$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=500\text{mA}$	1.58	-	-	-	nC
$Q_G(\text{TOT})$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}$	-	-	1.2	-	nC
$Q_{GS}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=500\text{mA}$	0.17	-	-	-	nC
$Q_{GS}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}$	-	-	0.24	-	nC
$Q_{GD}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=500\text{mA}$	0.24	-	-	-	nC
$Q_{GD}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=200\text{mA}$	-	-	0.36	-	nC
$C_{rss}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$	-	20	-	20	pF
$C_{iss}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$	-	150	-	175	pF
$C_{oss}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$	-	25	-	30	pF
$t_{on}$	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=540\text{mA}, R_G=10\Omega$	10	-	-	-	ns
$t_{off}$	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=540\text{mA}, R_G=10\Omega$	25	-	-	-	ns
$t_{on}$	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=215\text{mA}, R_G=10\Omega$	-	-	22	-	ns
$t_{off}$	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=215\text{mA}, R_G=10\Omega$	-	-	55	-	ns

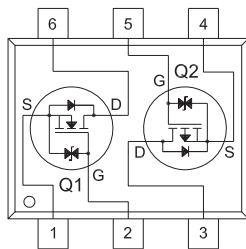
**SOT-563 - MECHANICAL OUTLINE**



SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.004	0.007	0.10	0.18
B	0.008		0.20	
C	0.022	0.024	0.56	0.60
D	0.059	0.067	1.50	1.70
E	0.020		0.50	
F	0.061	0.067	1.55	1.70
G	0.047		1.20	
H	0.006	0.012	0.15	0.30

SOT-563 (REV: R0)

**PIN CONFIGURATION**



**LEAD CODE:**

- 1) SOURCE Q1
- 2) GATE Q1
- 3) DRAIN Q2
- 4) SOURCE Q2
- 5) GATE Q2
- 6) DRAIN Q1

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